AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A system for generating a first clock frequency for a plurality of data bursts compressed in time, the system comprising:

a transmitter for transmitting a composite stream using the data bursts clocked at a second clock frequency; and

a receiver comprising a demultiplexer, said receiver for acquiring said composite stream, and said demultiplexer comprising a phase locked loop for generating the first clock frequency using said second clock frequency.

2. (Original) The system of claim 1, wherein said second clock frequency is higher than the first clock frequency.

3. (Previously Presented) The system of claim 1, wherein said de-multiplexer outputs the data bursts at the first clock frequency.

4. (Previously Presented) The system of claim 1, wherein said de-multiplexer includes a FIFO circuit.

5. (Cancelled)

6. (Previously Presented) The system of claim 25, wherein said digital phase locked loop comprises a second order feedback loop.

7. (Original) The system of claim 6, wherein said second order feedback loop comprises a half period calculator circuit.

8-24. (Cancelled)

25. (Previously Presented) The system of claim 1 wherein said phase locked loop comprises a digital phase locked loop.

26. (Amended) A system for generating a first clock frequency for a plurality of data bursts compressed in time, the system comprising:

a transmitter for transmitting a composite stream using the data bursts clocked at a second clock frequency; and

a receiver comprising a demultiplexer, said receiver for acquiring said composite stream, and said demultiplexer comprising at least a second order feedback loop for ~~generating~~ determining a period of the first clock frequency.

27. (Previously Presented) The system of claim 26, wherein said second clock frequency is higher than the first clock frequency.

28. (Previously Presented) The system of claim 26, wherein said de-multiplexer outputs the data bursts at the first clock frequency.

29. (Previously Presented) The system of claim 26, wherein said de-multiplexer comprises a FIFO circuit.

30. (Amended) A system for generating a first clock frequency for a plurality of data bursts compressed in time, the system comprising:

a transmitter for transmitting a composite stream using the data bursts clocked at a second clock frequency; and

a receiver comprising a demultiplexer, said receiver for acquiring said composite stream, and said demultiplexer comprising at least ~~a second order feedback loop having~~ a half period calculator circuit for generating at least one full cycle of the first clock frequency.

31. (Previously Presented) The system of claim 30, wherein said second clock frequency is higher than the first clock frequency.

32. (Previously Presented) The system of claim 30, wherein said demultiplexer outputs the data bursts at the first clock frequency.

33. (Previously Presented) The system of claim 30, wherein said de-multiplexer comprises a FIFO circuit.

34. (Previously Presented) A system for generating a first clock frequency for a plurality of data bursts compressed in time, the system comprising:

means for acquiring a composite stream formed using a second clock frequency;

means for determining the first clock frequency using said second clock frequency, said determining means including at least a digital phase locked loop.

35. (Previously Presented) The system of claim 34, comprising means for forming said composite stream.

36. (Previously Presented) The system of claim 35, wherein said forming means comprises a transmitter.

37. (Previously Presented) The system of claim 34, wherein said second clock frequency is higher than the first clock frequency.

38. (Previously Presented) The system of claim 34, wherein said determining means outputs the data bursts at the first clock frequency.

39. (Previously Presented) The system of claim 34, wherein said determining means comprises a FIFO circuit.

40. (Previously Presented) The system of claim 34, wherein said digital phase locked loop comprises a second order feedback loop.

41. (Previously Presented) The system of claim 46, wherein said second order feedback loop comprises a half period calculator circuit.

42. (Previously Presented) A method of generating a first clock frequency for a plurality of data bursts compressed in time, the method comprising:

acquiring a composite stream including at least the data bursts clocked at a second clock frequency; and

generating the first clock frequency using a digital phase locked loop and said second clock frequency.

43. (Previously Presented) The method of Claim 42 comprising transmitting said composite stream using the data bursts clocked at said second clock frequency.

44. (Original) The method of claim 42, wherein said second clock frequency is higher than the first clock frequency.

45. (Previously Presented) The method of claim 42 comprising outputting the data bursts at the first clock frequency.

46. (Previously Presented) The method of claim 42, wherein said digital phase locked loop comprises a second order feedback loop.

47. (Previously Presented) The method of claim 42, wherein said second order feedback loop comprises a half period calculator circuit.

48. (Previously Presented) A method of generating a first clock frequency for a plurality of data bursts compressed in time, the method comprising:

transmitting a composite stream and the data bursts clocked at a second clock frequency;

acquiring said composite stream; and

generating the first clock frequency using a demultiplexer, said demultiplexer having a digital phase locked loop that generates the first clock frequency using said second clock frequency.

49. (Original) The method of claim 48, wherein said second clock frequency is higher than the first clock frequency.

50. (Previously Presented) The method of claim 48 comprising outputting the data bursts at the first clock frequency.

51. (Previously Presented) The method of claim 48, wherein said digital phase locked loop comprises a second order feedback loop.

52. (Previously Presented) The method of claim 51, wherein said second order feedback loop comprises a half period calculator circuit.

53. (Amended) A method of generating a first clock frequency for a plurality of data bursts compressed in time, the method comprising:

acquiring a composite stream using the data bursts clocked at a second clock frequency; and

generating <u>at least one full cycle of</u> the first clock frequency using at least a half period calculator circuit and said second clock frequency.

54. (Previously Presented) The method of Claim 53 comprising transmitting said composite stream using the data bursts clocked at said second clock frequency.

55. (Original) The method of claim 53, wherein said second clock frequency is higher than the first clock frequency.

56. (Previously Presented) The method of claim 53 comprising outputting the data bursts at the first clock frequency.

57. (Amended) A method of generating a first clock frequency for a plurality of data bursts compressed in time, the method comprising:

acquiring a composite stream using the data bursts clocked at a second clock frequency; and

~~generating~~ determining a period of the first clock frequency using at least a second order feedback loop and said second clock frequency.

58. (Previously Presented) The method of Claim 57 comprising transmitting said composite stream using the data bursts clocked at said second clock frequency.

59. (Original) The method of claim 57, wherein said second clock frequency is higher than the first clock frequency.

60. (Previously Presented) The method of claim 57 comprising outputting the data bursts at the first clock frequency.